

CLAIMS:

1. Bit-detection arrangement able to convert an analog signal (AS) having an amplitude into a digital signal (DS) representing a bit sequence from which the analog signal (AS) is derived, comprising:
 - a quantizer (11) able to produce an output signal S_1 by quantizing the amplitude of the analog signal (AS), and
 - a phase detector PD_1 (12) able to determine a phase difference ΔP_1 between the output signal S_1 and a clock signal C_2 , and able to generate an output signal PH_2 having an amplitude, where the amplitude of PH_2 indicates the phase difference ΔP_1 ,
 - an analog to digital converter ADC (13) which is able to output a processed signal (PrS) by sampling the output signal PH_2 at a sample rate controlled by a clock signal C_1 having a frequency which is equal to the frequency of clock signal C_2 divided by a factor n ,
 - a digital phase locked loop DPLL (2) able to lock on the processed signal (PrS) and able to output a phase signal PH_1 using the clock signal C_1 , and
 - a bit decision unit (3) able to output the digital signal (DS) and a clock signal C_3 using the phase signal PH_1 , the clock signal C_1 and the output signal S_1 , comprising a sample and hold unit SH_1 able to sample the output signal S_1 , using a clock signal C_{SH1} having a frequency equal to the frequency of clock signal C_2 , and to hold n samples, $sample_{y=1}$ through $sample_{y=n}$, of the output signal S_1 for a clock period of clock signal C_1 , n being the division factor of clock signal C_2 , where n is an integer greater than one, characterized in that the bit decision unit further comprises
 - at least one additional sample and hold unit SH_2 able to sample the output signal S_1 , using a clock signal C_{SH2} and wherein the frequency of the clock signal C_{SH2} is equal to the frequency of clock signal C_{SH1} and the phase of clock signal C_{SH2} is substantially different from the phase of clock signal C_{SH1} , and
 - an output unit for outputting samples of either the sample and hold units SH_1 or SH_2 , wherein the samples of the sample and hold unit SH_1 are outputted when the phase signal PH_1 indicates that the phase difference ΔP_1 is in a first region and the samples of the

additional sample and hold unit SH_2 are outputted when the phase signal PH_1 indicates that the phase difference ΔP_1 is in a second region.

2. Bit-detection arrangement as claimed in claim 1, characterized in that the
5 phase difference between clock signal C_{SH1} and clock signal C_{SH2} is approximately 180 degrees and the phase of clock signal C_{SH1} is approximately equal to the phase of clock signal C_2 and wherein in the first region the phase difference ΔP_1 is between 0 degrees and 90 degrees and in the second region the phase difference ΔP_1 is between 90 degrees and 180 degrees.
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3. Bit-detection arrangement as claimed in claim 1 or 2, characterized in that the bit decision unit further comprises sample and hold units SH_3 through SH_x , wherein the sample and hold units SH_1 through SH_x are clocked by clock signals C_{SH1} through C_x , wherein the frequency of the clock signals C_{SH2} through C_{SHx} is equal to the frequency of
15 clock signal C_{SH1} and the phases of the clock signals C_{SH1} through C_{SHx} are substantially different from each other and in that the output unit is adapted to output samples of the sample and hold units SH_1 through SH_x , wherein the phase signal PH_1 is divided into x regions, x being the number of sample and hold units, and wherein the output unit is able to output samples of the sample and hold unit which corresponds to the region in which the
20 current value of the phase signal PH_1 resides.
4. Bit-detection arrangement as claimed in claim 1, characterized in that the bit detection unit further comprises a clock signal selection unit for outputting the clock signal C_{SH1} and clock signal C_{SH2} wherein the clock signal selection unit is able to change the
25 phases of the clock signals C_{SH1} and C_{SH2} in dependence of the current value of the phase signal PH_1 .
5. Bit-detection arrangement as claimed in claim 4, characterized in that the clock signal selection unit is fed with clock signals C_n through C_k having a frequency equal
30 to clock signal C_2 and wherein the phases of the clock signals C_n through C_k differ from each other, and wherein the clock signal selection unit passes two of the clock signals C_n through C_k through as the clock signals C_{SH1} and C_{SH2} in dependence of the phase signal PH_1 .

6. Apparatus for reproducing information recorded on an information carrier, provided with the bit-detection arrangement as claimed in one of the previous claims.